REMARKS

This application has been carefully reviewed in light of the Office Action dated October 7, 2002. Applicants have amended claims 1, 5, 6, 8, 9, and 13. Reconsideration and favorable action in this case are respectfully requested.

The Examiner has objected to the specification for having reference numerals in the Abstract. Applicants have amended the specification accordingly. Applicants have also corrected a grammatical error in the Abstract.

The Examiner has objected to claims 1, 5, 7 and 8. Applicants have amended claims 1, 5, and 8. While the Examiner stated that "cell" should be pluralized in claim 7, Applicants believe that the Examiner meant to reference claim 8 for this informality and has appropriately amended this claim.

The Examiner has rejected claims 6, 9 and 13 under 35 U.S.C. §112, second paragraph. Applicants have amended the claims in accordance with the Examiner's concerns.

The Examiner has also rejected claims under 35 U.S.C. §102(b) as being unpatentable over U.S. Pat. No. 5,838,583 to Varadarajan et al (hereinafter "Varadarajan"). Applicants have reviewed this reference in detail and do not believe that it discloses or makes obvious the invention as claimed.

In the present invention, an integrated circuit design includes datapath cells in a structured layout and other cells in an unstructured layout. A description of a desired layout for the datapath cells is generated and transferred to a place and route tool, in order to assign the desired layout to the datapath cells within the place and route tool. The datapath cells are assigned a predetermined status to prevent movement of the cells. Constraint information regarding the other cells is then transferred to the place and route tool and optimization procedures may be performed on the layout based on desired

criteria, such that the datapath cells are unmoved as different layout iterations are performed on the other cells.

The Varadarajan reference does not show the use of a fixed status to fix the placement of the datapath cells prior to optimization of the other cells, as provided in independent claims 1 and 8. The use of the fixed status to fix the placement of the datapath cells allows the circuit designer to carefully and flexibly place critical structured logic in a desired arrangement that will not be affected by subsequent optimization routines for the other cells. With the structure logic fixed, the place and route tool can efficiently iterate through all possible placements of the other cells (leaving the placement of the datapath cells unchanged) to find an optimum solution.

Applicants have reviewed the Varadarajan reference, and have specifically reviewed column 3, lines 52 through column 4, line 28, for a teaching regarding using a fixed status to datapath cells, but did not find any such teaching.

Accordingly, Applicants respectfully request allowance of independent claims 1 and 8.

Since claims 2-7 and 9-15 are dependent upon claims 1 and 8, Applicant respectfully request allowance thereof.

An extension of one month is requested and a Request for Extension of Time under § 1.136 with the appropriate fee is attached hereto.

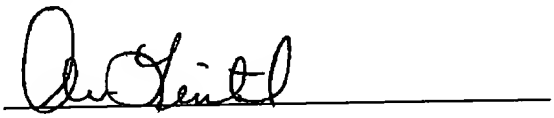
The Commissioner is hereby authorized to charge any fees or credit any overpayment, including extension fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it

is respectfully requested that the Examiner telephone Alan W. Lintel, Applicants' Attorney at (972) 664-9595 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



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Version with marking to show changes made:

In the specification:

A layout system [(10)] includes a place and route tool [(12)] and a datapath layout generator. The datapath layout generator [(14)] provides a mechanism for the designer to place datapath cells in a structured arrangement. The datapath layout generator [(14)] sends a language configuration file to the place and route tool [(12)] to install the datapath structure. The datapath structure is assigned "fixed" status, which prevents the place and route tool [(12)] from moving the datapath cells in later operations. Constraints for the remaining cells are then installed in the place and route tool [(12)], and criteria-driven placement, such as timing-driven placement, can be used to arrange these cells in an optimum fashion. The remaining cells can be placed in open areas of the datapath structure for improved density.

In the claims

1 (Amended). A method of controlling layout of [cell] cells in an integrated circuit including datapath cells in a structured layout and other cells in an unstructured layout, comprising the steps of:

generating a description of a desired layout for the datapath cells;

transferring said description to a place and route tool to assign the desired layout to the datapath cells within the place and route tool;

assigning a fixed status to the datapath cells to prevent movement of the cells;

transferring desired criteria regarding the other cells to the place and route tool; and

optimizing the layout based on said desired criteria, such that the datapaths cells are unmoved as different layout iterations are performed on the other cells.

5 (Amended). The method of claim 3 wherein said step of generating one or more matrices comprises the step of generating matrices having two or more matrices with interleaved columns.

6 (Amended). The method of claim 3 wherein said step of generating matrices comprises the step of generating matrices leaving free space between slots for datapath cells in which ones of said other cells [may be] are placed.

8 (Amended). An [Apparatus] apparatus for controlling layout of [cell] cells in an integrated circuit including datapath cells in a structured layout and other cells in an unstructured layout, comprising:

a place and route tool;

a datapath generator for generating a description of a desired layout for the datapath cells and transferring said description to a place and route tool to assign the desired layout to the datapath cells within the place and route tool;

wherein a fixed status can be assigned to the datapath cells in said place and route tool to prevent movement of the cells during optimization of the layout of said other cells.

9 (Amended). The apparatus of claim 8 wherein said place and route tool [may receive] receives information on said datapath and other cells.

13 (Amended). The apparatus of claim 10 wherein said datapath generator generates a description of a plurality of matrices for datapath cells leaving free space between slots of said matrices in which ones of said other cells [may be] are placed.